



PTO/SB/08A (08-03)

Substitute for form 1449A/PTO		Complete if Known			
		Application Number	10/798,597		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Date	March 10, 2004		
		First Named Inventor	Xiaobao Wang		
		Art Unit	Unassigned		
		Examiner Name	Unassigned		
Sheet	1	of	3	Attorney Docket Number	015114-054911US

U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	1	US-6,489,837	12-03-2002	Schultz et al.	
	2	US-6,466,063 B2	10-15-2002	Chen	
	3	US-6,448,813 B2	09-10-2002	Garlepp et al.	
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	41	US-5,134,311	07-28-1992	Biber et al.	

Examiner Signature		Date Considered	9/1/05
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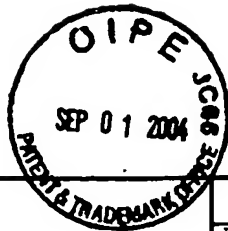
U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. ¹	Document Number Number Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		Country Code ³	Number ⁴	Kind Code ⁵ (If known)				

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PTO/SB/08B (08-03)

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				Filing Date	March 10, 2004
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				Art Unit	Unassigned
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Sheet	3	of	3	Attorney Docket Number	015114-054911US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>De</i>	45	"Apex 20K Programmable Logic Device Family," product data sheet, version 3.7, May 2001 Altera Corporation San Jose, CA (2001), pp. 1-8, pp. 37-47.	
<i>De</i>	46	"Apex II Programmable Logic Device Family," product data sheet, version 1.1, May 2001 Altera Corporation San Jose, CA (2001), pp. 1-8, pp. 38-59	
<i>De</i>	47	"Virtex-II 1.5V Field Programmable Gate Arrays," product specifications DSO3102 (v1.5) April 2, 2001., Xilinx, Inc., San Jose, CA (2001), pp. 1-36	
<i>De</i>	48	BENDAK et al. "CMOS VLSI Implementation of Gigabyte/second computer network links," proceedings of the IEEE International Symposium on Circuits and Systems '96, pp. 269-272 (1996).	
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<i>De</i>	50	ESCH et al. "Theory and Design of CMOS HSTL I/O Pads," The Hewlett Packard Journal (1998), pp. 46-52	

Examiner Signature	<i>Paul D. Chany</i>	Date Considered	9/1/05
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